

**Notice of References Cited**

Application/Control No.

09/510,203

Applicant(s)/Patent Under  
Reexamination  
FIELDS ET AL.

Examiner

Ayal I Sharon

Art Unit

2123

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,223,326	04-2001	Fields et al.	716/4
	B	US-5,995,736	11-1999	Aleksic et al.	716/18
	C	US-5,673,199	09-1997	Gentry, Roy M.	703/1
	D	US-5,752,002	05-1998	Naidu et al.	703/14
	E	US-6,539,522	03-2003	Devins et al.	716/5
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Fields, C.A. "Creating Hierarchy in HDL-Based High Density FPGA Design". Proceedings EURO-DAC '95. Sept. 18-22, 1995. pp.594-599.
	V	Doughty, F. "6.111 Introductory Digital Systems Laboratory". Emacs Help page. Jan. 18, 2000. <a href="http://sunpal2.mit.edu/6.111">http://sunpal2.mit.edu/6.111</a>
	W	"Welcome to Digital Signal Processing Support" - "Intro. to Synopsys to XACT M1 Design Flow", Sept. 6, 1999. <a href="http://www.ee.qub.ac.uk/dsp/support/documentation/synopsys_to_xact/intro_synopsys_xact.html">http://www.ee.qub.ac.uk/dsp/support/documentation/synopsys_to_xact/intro_synopsys_xact.html</a>
	X	Poterie, B. "Storage Mechanism for VHDL Intermediate Form", Proceedings of the European Design Automation Conference (EDAC), 1990. March 12-15, 1990. pp.506-510.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.